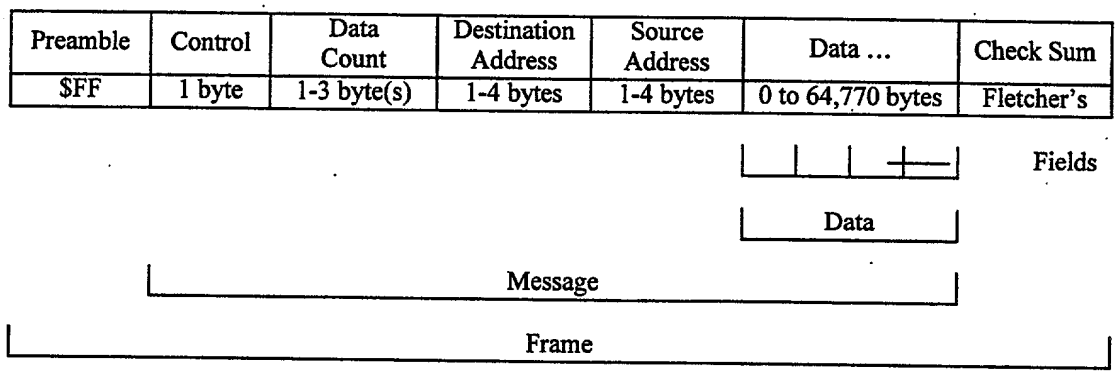
Preamble
Control
Data Count
Destination Address
Source Address
Data ...
Check Sum
$FF
1 byte
1-3 byte(s)
1-4 bytes
1-4 bytes
0 to 64,770 bytes
Fletcher's
Fields
Data
Message
Frame

FIG. 1

Bit 7	Reserved for future use, must be zero.
Bit 6	Reserved for future use, must be zero.
Bit 5	Reserved for future use, must be zero.
Bit 4	Response bit. Indicates that this message is a response to another device's request.
Bit 3	Response Required bit. The "Response Required" bit is used by any device that wishes a response from another device in the system.
Bit 2	Bus Grant. If this bit is on, the token (right to control access to the transmission media) is passed to the next device in sequence. If the bit is off, the current bus master retains control.
Bit 1 Bit 0	Address Mode. If these bits are both zero (00) then the frame includes a single byte for destination address and a single byte for the source address. If the low bit is on (01) then the destination and source addresses are two bytes each. If the upper bit is on (10) then there are three address bytes and (obviously) if both bits are on, there are four bytes each for destination and source.

FIG. 2

Response Required Bit	Bus Grant Bit	Meaning
0	0	No response to this message is expected and the transmitter is not releasing control over the transmission medium.
0	1	No response to this message is expected and the transmitter is releasing control over the transmission medium.
1	0	A response to this message is expected and the transmitter is not releasing control over the transmission medium. This means that the responding device must respond immediately. This combination is acceptable only between peers on a local bus. To get responses from devices on remote buses, see the combination below (1,1).
1	1	A response to this message is expected and the transmitter is releasing control over the bus to another device. This means that the device responding must hold it's response until it obtains the right to use the bus. The local bus will continue with it's normal token passing.

FIG. 3

Byte 4	Byte 3	Byte 2	Byte 1
Backbone	Hub	Bus	Device

FIG. 4

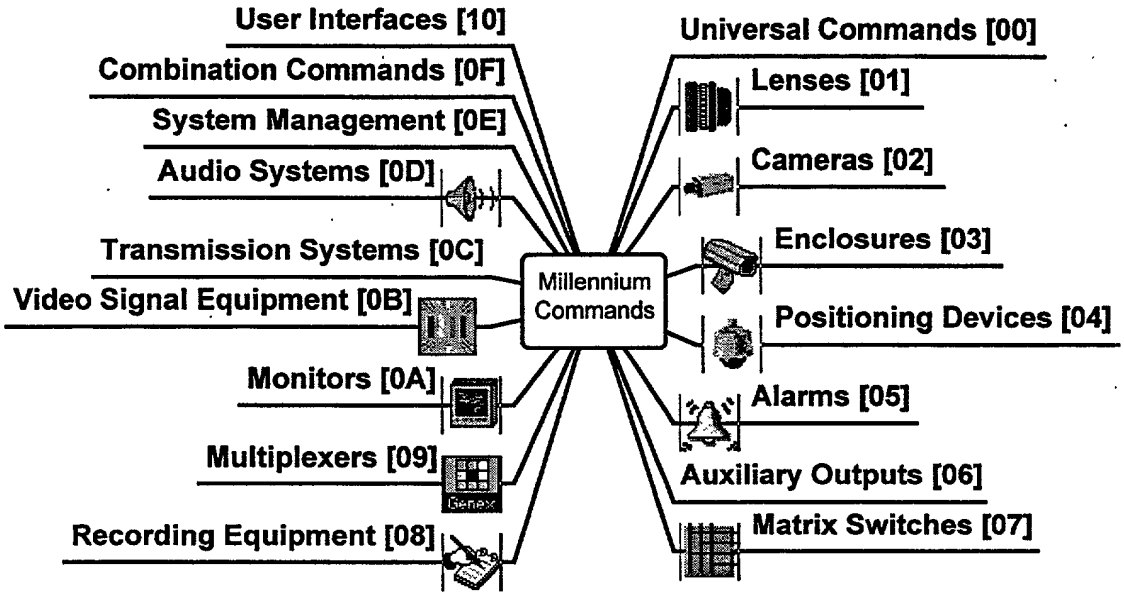

FIG. 5

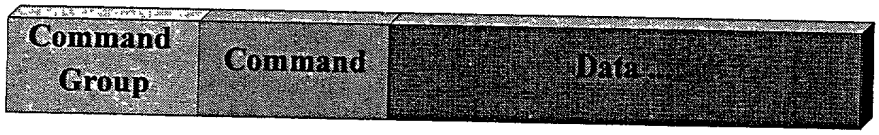

FIG. 6

$$C(0) = \left(\sum_{i=1}^{n} B(i) \right) \bmod 256$$

$$C(1) = \left(\sum_{i=1}^{n} C(0) \right) \bmod 256$$

FIG. 7

Undetected Error Type	CRC	Fletcher's 1's Compliment	Fletcher's 2's Compliment
% of all errors missed	.001526	.001538	.001526
% of 16 bit burst errors missed	none	.000019	None
% single bit errors missed	none	none	None
Minimum separation of undetected 2 bit errors	65535	2040	16

FIG. 8

Message to transmit	05	C0	AA	FF	37	FF	FD	A7	FF	FF	FE	FD
After Byte Stuffing	05	C0	AA	FE	FE	37	FE	FD	FD	A7	FE	FE	FE	FE	FE	FD	FD

FIG. 9

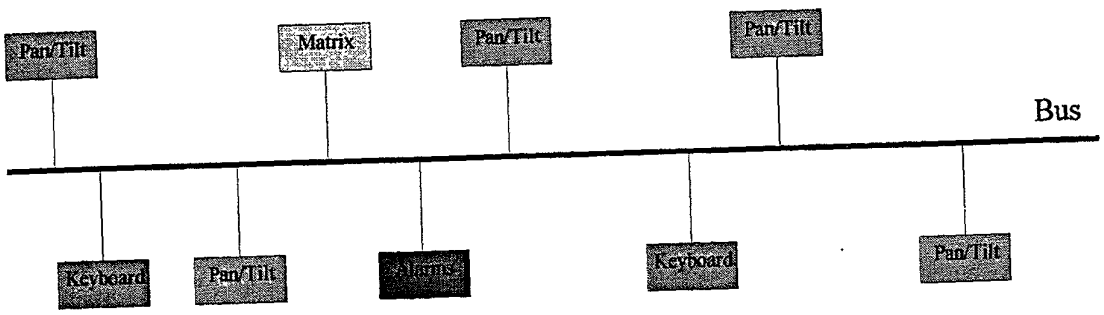

FIG. 10

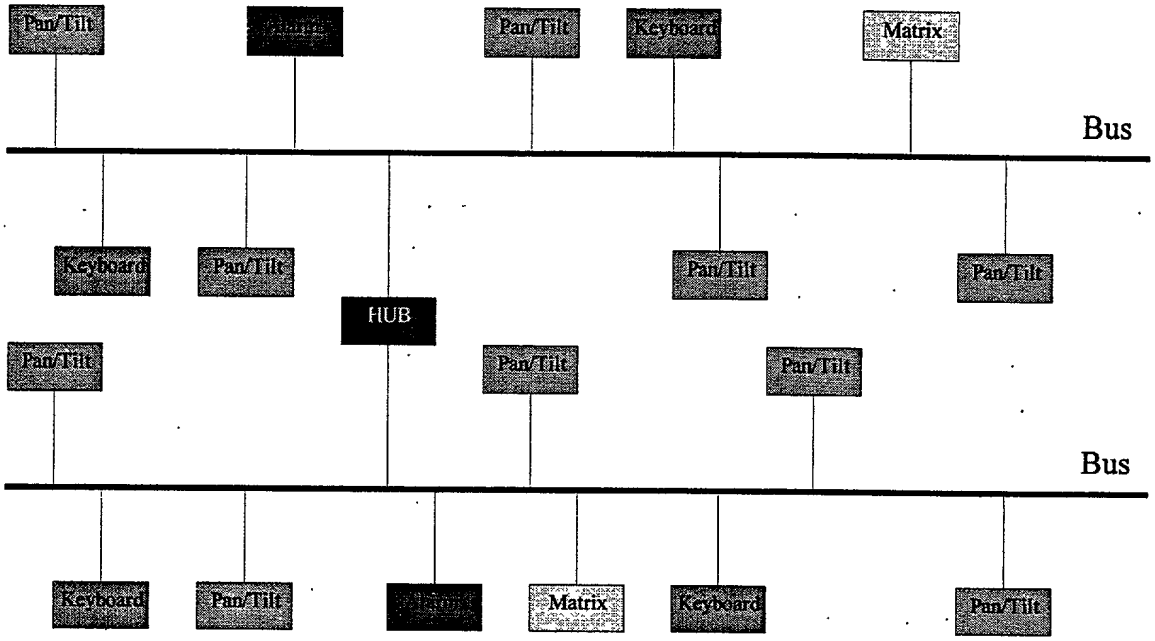
Pan/Tilt
Keyboard
Pan/Tilt
Keyboard
Matrix
Bus
Keyboard
Pan/Tilt
HUB
Pan/Tilt
Pan/Tilt
Pan/Tilt
Pan/Tilt
Pan/Tilt
Bus
Keyboard
Pan/Tilt
Matrix
Keyboard
Pan/Tilt

FIG. 11

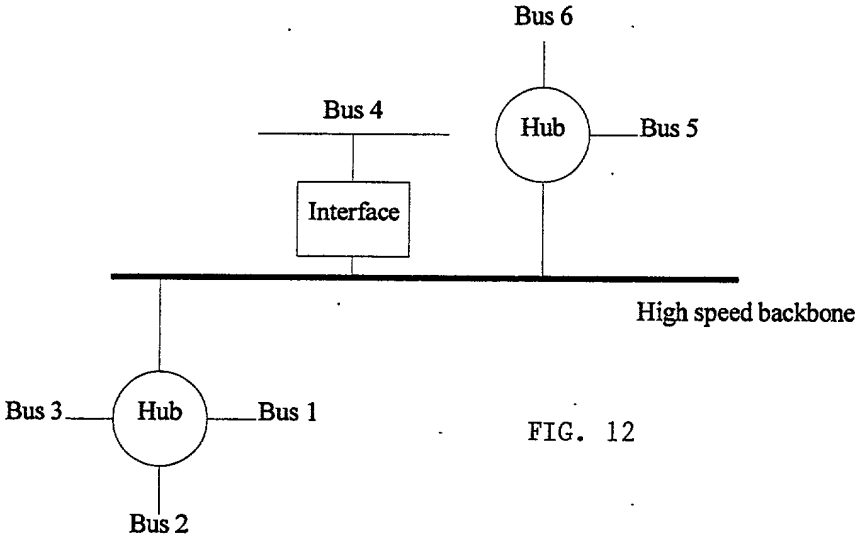
Bus 6
Bus 4
Hub
Bus 5
Interface
High speed backbone
Bus 3
Hub
Bus 1
Bus 2

FIG. 12

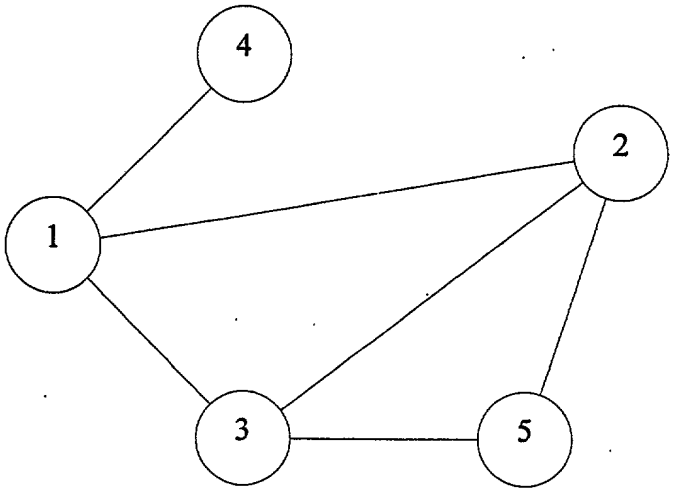

FIG. 13

		TO				
		1	2	3	4	5
FROM	1		X	X	X	
	2	X		X		X
	3	X	X			X
	4	X				
	5		X	X		

FIG. 14